Abstract. The modern communication technologies require the use of CMOS monolithic oscillators because of their small manufacturing costs and high integration capabilities. The disadvantages of CMOS ring oscillators can be compensated through the use of a VCO architecture. The control voltage of this VCO should compensate for the frequency drift due to process and temperature.

1 Introduction

Although the more common quartz crystal oscillators is still preferred because of the stability with variations in supply voltage, temperature and process recent advances in the compensation techniques transform the integrated CMOS ring oscillator into a suitable replacement. Without any compensation scheme the central frequency drift of the CMOS oscillator can be up to 100% when the temperature is varied. The process corners also influence the central frequency of an oscillator. Process corners are determined by variations in oxide thickness, threshold voltage and deviations of the physical dimensions of the transistor (dW and dL). In this paper an on-chip ring oscillator is considered. The compensation can be done through the use of a simple microcontroller that has a DAC an ADC and a temperature sensor. The digital part of the voltage generation is simulated in the Cadence environment using a Verilog model for the control voltage generator. This voltage generator accounts not only for the Fast n-channel, Fast p-channel (FF) and Slow n-channel, Slow p-channel (SS) corners but also for the Fast n-channel, Slow p-channel (FS) and Slow n-channel, Fast p-channel (SF).

2 The Ring Oscillator

The ring oscillator considered has 4 differential delay cells; the first 3 cells are in a inverting connexion and the fourth is connected as a buffer. Using this connexion scheme (Fig1) 4 signals with 0°, 90°, 180°, 270° phase shift are generated.

Figure 1: Oscillator core.

The differential delay cell is based on the delay cell proposed by Maneatis [1] and [2], (Fig. 2). The biasing of the circuit is done using a half buffer replica boosted dynamic bias (Fig 3) in order to reduce the supply noise [3]. Two half buffer circuits are used in order to isolate the control voltage input from the gate of the PMOS transistors in the oscillator.
Figure 2: Delay cell [1].

Between the bias points of the PMOS and NMOS a bypass capacitor is introduced in order to prevent oscillations.

Figure 3: Bias circuit.

The output frequency of the ring oscillator is approximately represented in (1)

\[
F = \frac{I_d}{2NC_oV_{SW}} = \frac{k_pI_p(V_{ref} - V_{TP} - V_{ctrl})^2}{2NC_o(V_{ref} - V_{ctrl})}
\]  

(1)

3 Compensation of the ring oscillator

We want to see what happens when a temperature variation occurs. From the Bsim3.3V model [4] the threshold voltage has a linear variation with the temperature

\[
V_{TP} = V_{TP0} + kT \left( \frac{T}{T_0} - 1 \right)
\]  

(2)

where \( kT \) has a negative value.

The electron mobility also varies with the temperature

\[
\mu(T) = \mu_0 \left( \frac{T}{T_0} \right)^n
\]  

(3)
Considering $C_{OX}$ temperature variation the same as for the output capacitance, then:

$$F = \frac{\mu p_0 T_0}{2 N C_O} \left( V_{ref} - V_{Tp0} - V_{ctl} + \frac{kt}{T_0} \right)^2$$

In Fig 4 the schematic of the corner detector is presented. The output voltage of this detector varies with temperature and process. An NMOS threshold detector architecture is preferred to the PMOS architecture presented in [5] and [6] because the generated values are unique.

Figure 4: Process corner detector and output voltage.

Using this detector the corner is detected and the appropriate slope for the voltage can be generated.

4 Results
The oscillator was designed using the 90nm GPDK in Cadence. The supply voltage was set at 2.2V and the central frequency of the oscillator is 1GHz, Fig 5. The circuit draws a current of about 10mA so the power consumption without the control circuit of the circuit is about 22mW which qualifies the circuit as low power. In order to compensate the frequency across temperature and process the control voltage must take values between 0.7V and 1.5V. Using a resolution of 10mV a compensation of ± 3% is obtained over corners and a temperature variation of 0°-80°. This can be obtained using a 8-Bit DAC.
5 Conclusions

- In this paper a digital technique for the compensation of a ring oscillator is proposed.
- A Verilog model is used in order to simulate the digital part of the circuit.
- The proposed solution does not require calibration because the circuit generates the correct control voltage based on the output voltage of the threshold detector and the temperature reading.
- A variation of ± 3% is obtained over the temperature range of 0°-80° and the 4 corners.

References